High Precision, Wideband RMS-to-DC Converter

AD637

FEATURES

High accuracy
- **0.02% max nonlinearity, 0 V to 2 V rms input**
- **0.10% additional error to crest factor of 3**

Wide bandwidth
- **8 MHz at 2 V rms input**
- **600 kHz at 100 mV rms**

Computes
- **True rms**
- **Square**
- **Mean square**
- **Absolute value**

dB output (60 dB range)

Chip select/power-down feature allows
- **Analog three-state operation**
- **Quiescent current reduction from 2.2 mA to 350 µA**

14-lead SBDIP, 14-lead low cost CERDIP, and 16-lead SOIC_W

FUNCTIONAL BLOCK DIAGRAM

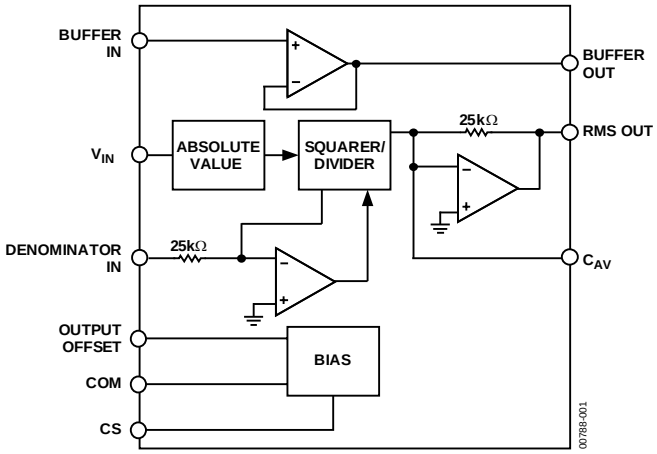

Figure 1. SBDIP (D-14) and CERDIP (Q-14) Packages

GENERAL DESCRIPTION

The AD637 is a complete high accuracy, monolithic rms-to-dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms-to-dc converters and comparable to discrete and modular techniques in accuracy, bandwidth, and dynamic range. A crest factor compensation scheme in the AD637 permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The circuit's wide bandwidth permits the measurement of signals up to 600 kHz with inputs of 200 mV rms and up to 8 MHz when the input levels are above 1 V rms.

As with previous monolithic rms converters from ADI, the AD637 has an auxiliary dB output available to the user. The logarithm of the rms output signal is brought out to a separate pin, allowing direct dB measurement with a useful range of 60 dB. An externally programmed reference current allows the user to select the 0 dB reference voltage to correspond to any level between 0.1 V and 2.0 V rms.

A chip select connection on the AD637 permits the user to decrease the supply current from 2.2 mA to 350 µA during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or hand-held applications where minimum power consumption is critical. In addition, when the AD637 is powered down, the output goes to a high impedance state. This allows several AD637s to be tied together to form a wideband true rms multiplexer.

The input circuitry of the AD637 is protected from overload voltages that are in excess of the supply levels. The inputs are not damaged by input signals if the supply voltages are lost.

The AD637 is available in Accuracy Grades J and K for commercial temperature range (0°C to 70°C) applications; Accuracy Grades A and B for industrial range (−40°C to +85°C) applications; and Accuracy Grade S rated over the −55°C to +125°C temperature range. All versions are available in hermetically sealed, 14-lead SBDIP, 14-lead CERDIP, and 16-lead SOIC packages.

The AD637 computes the true root-mean-square, mean-square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal since it relates directly to the power of the signal. The rms value of a statistical signal is also related to the standard deviation of the signal.

The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor that sets the averaging time period. The value of this capacitor also determines low frequency accuracy, ripple level, and settling time.

The on-chip buffer amplifier can be used either as an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby increasing accuracy.

Rev. G

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SPECIFICATIONS[1]

At 25°C, and ±15 V dc unless otherwise noted.

Table 1.

Parameter	AD637J/ AD637A Min	AD637J/ AD637A Typ	AD637J/ AD637A Max	AD637K/ AD637B Min	AD637K/ AD637B Typ	AD637K/ AD637B Max	AD637S Min	AD637S Typ	AD637S Max	Unit
TRANSFER FUNCTION	$V_{OUT} = \sqrt{avg \times (V_{IN})2}$									
CONVERSION ACCURACY										
Total Error, Internal Trim[2] (Figure 5)			**±1 ± 0.5**			**±0.5 ± 0.2**			**±1 ± 0.5**	mV ±% of reading
T_{MIN} to T_{MAX}			**±3.0 ± 0.6**			**±2.0 ± 0.3**			**±6 ± 0.7**	mV ± % of reading
vs. Supply, $+V_{IN}$ = +300 mV		30	**150**		30	**150**		30	**150**	µV/V
vs. Supply, $-V_{IN}$ = −300 mV		100	**300**		100	**300**		100	**300**	µV/V
DC Reversal Error at 2 V			**0.25**			**0.1**			**0.25**	% of reading
Nonlinearity 2 V Full Scale[3]			**0.04**			**0.02**			**0.04**	% of FSR
Nonlinearity 7 V Full Scale			**0.05**			**0.05**			**0.05**	% of FSR
Total Error, External Trim		±0.5 ± 0.1			±0.25 ± 0.05			±0.5 ± 0.1		mV ± % of reading
ERROR VS. CREST FACTOR[4]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		±0.1			±0.1			±0.1		% of reading
Crest Factor = 10		±1.0			±1.0			±1.0		% of reading
AVERAGING TIME CONSTANT		25			25			25		ms/µF C_{AV}
INPUT CHARACTERISTICS										
Signal Range, ±15 V Supply										
Continuous RMS Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±15			±15			±15	V p-p
Signal Range, ±5 V Supply										
Continuous RMS Level		0 to 4			0 to 4			0 to 4		V rms
Peak Transient Input			±6			±6			±6	V p-p
Maximum Continuous Nondestructive Input Level (All Supply Voltages)			±15			±15			±15	V p-p
Input Resistance	6.4	8	9.6	6.4	8	9.6	6.4	8	9.6	kΩ
Input Offset Voltage			±0.5			±0.2			±0.5	mV

Parameter	AD637J/AD637A Min	AD637J/AD637A Typ	AD637J/AD637A Max	AD637K/AD637B Min	AD637K/AD637B Typ	AD637K/AD637B Max	AD637S Min	AD637S Typ	AD637S Max	Unit
FREQUENCY RESPONSE[5]										
Bandwidth for 1% Additional Error (0.09 dB)										
V_{IN} = 20 mV		11			11			11		kHz
V_{IN} = 200 mV		66			66			66		kHz
V_{IN} = 2 V		200			200			200		kHz
±3 dB Bandwidth										
V_{IN} = 20 mV		150			150			150		kHz
V_{IN} = 200 mV		1			1			1		MHz
V_{IN} = 2 V		8			8			8		MHz
OUTPUT CHARACTERISTICS										
Offset Voltage			**±1**			**±0.5**			**±1**	mV
vs. Temperature		±0.05	**±0.089**		±0.04	**±0.056**		±0.04	**±0.07**	mV/°C
Voltage Swing, ±15 V Supply, 2 kΩ Load	**0 to 12.0**	13.5		**0 to 12.0**	13.5		**0 to 12.0**	13.5		V
Voltage Swing, ±3 V Supply, 2 kΩ Load	**0 to 2**	2.2		**0 to 2**	2.2		**0 to 2**	2.2		V
Output Current	**6**			**6**			**6**			mA
Short-Circuit Current		20			20			20		mA
Resistance, Chip Select High		0.5			0.5			0.5		Ω
Resistance, Chip Select Low		100			100			100		kΩ
dB OUTPUT										
Error, V_{IN} 7 mV to 7 V rms, 0 dB = 1 V rms		±0.5			±0.3			±0.5		dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor Temperature Coefficient		+0.33			+0.33			+0.33		% of Reading/°C
		−0.033			−0.033			−0.033		dB/°C
I_{REF} for 0 dB = 1 V rms	5	20	**80**	5	20	**80**	5	20	**80**	µA
I_{REF} Range	1		100	1		100	1		100	µA
BUFFER AMPLIFIER										
Input Output Voltage Range	$-V_S$ to $(+V_S - 2.5\ V)$			$-V_S$ to $(+V_S - 2.5\ V)$			$-V_S$ to $(+V_S - 2.5\ V)$			V
Input Offset Voltage		±0.8	**±2**		±0.5	**±1**		±0.8	±**2**	mV
Input Current		±2	**±10**		±2	**±5**		±2	±**10**	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	−0.13		5	−0.13		5	−0.13		5	mA
Short Circuit Current		20			20			20		mA
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[6]		5			5			5		V/µs
DENOMINATOR INPUT										
Input Range		0 to 10			0 to 10			0 to 10		V
Input Resistance	20	25	30	20	25	30	20	25	30	kΩ
Offset Voltage		±0.2	±0.5		±0.2	±0.5		±0.2	±0.5	mV

Parameter	AD637J/ AD637A Min	AD637J/ AD637A Typ	AD637J/ AD637A Max	AD637K/ AD637B Min	AD637K/ AD637B Typ	AD637K/ AD637B Max	AD637S Min	AD637S Typ	AD637S Max	Unit
CHIP SELECT (CS)										
RMS ON Level	Open or 2.4 V < V_C < +V_S			Open or 2.4 V < V_C < +V_S			Open or 2.4 V < V_C < +V_S			
RMS OFF Level	V_C < 0.2 V		V_C < 0.2 V		V_C < 0.2 V					
I_{OUT} of Chip Select										
CS Low			10			10			10	µA
CS High			0			0			0	µA
On Time Constant		10 + ((25 kΩ) × C_{AV})			10 + ((25 kΩ) × C_{AV})			10 + ((25 kΩ) × C_{AV})		µs
Off Time Constant		10 + ((25 kΩ) × C_{AV})			10 + ((25 kΩ) × C_{AV})			10 + ((25 kΩ) × C_{AV})		µs
POWER SUPPLY										
Operating Voltage Range	**±3.0**		**±18**	**±3.0**		**±18**	**±3.0**		**±18**	V
Quiescent Current		2.2	**3**		2.2	**3**		2.2	**3**	mA
Standby Current		350	**450**		350	**450**		350	**450**	µA

[1] Specifications shown in **bold** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.
[2] Accuracy specified 0 V rms to 7 V rms dc with AD637 connected as shown in Figure 5.
[3] Nonlinearity is defined as the maximum deviation from the straight line connecting the readings at 10 mV and 2 V.
[4] Error vs. crest factor is specified as additional error for 1 V rms.
[5] Input voltages are expressed in volts rms. Percent is in % of reading.
[6] With external 2 kΩ pull-down resistor tied to $-V_S$.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
ESD Rating	500 V
Supply Voltage	±18 V dc
Internal Quiescent Power Dissipation	108 mW
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 10 secs)	300°C
Rated Operating Temperature Range	
AD637J, AD637K	0°C to 70°C
AD637A, AD637B	−40°C to +85°C
AD637S, 5962-8963701CA	−55°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

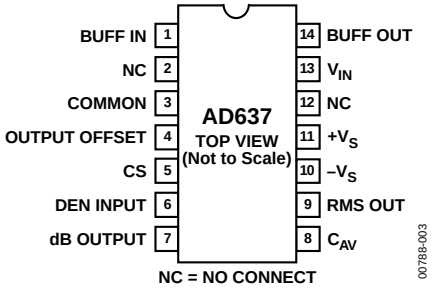


Figure 2. 14-Lead SBDIP/CERDIP Pin Configuration

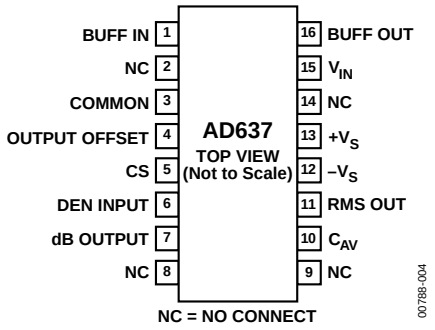


Figure 3. 16-Lead SOIC_W Pin Configuration

Table 3. 14-Lead SBDIP/CERDIP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BUFF IN	Buffer Input
2, 12	NC	No Connection
3	COMMON	Analog Common
4	OUTPUT OFFSET	Output Offset
5	CS	Chip Select
6	DEN INPUT	Denominator Input
7	dB OUTPUT	dB Output
8	C_{AV}	Averaging Capacitor Connection
9	RMS OUT	RMS Output
10	$-V_S$	Negative Supply Rail
11	$+V_S$	Positive Supply Rail
13	V_{IN}	Signal Input
14	BUFF OUT	Buffer Output

Table 4. 16-Lead SOIC_W Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BUFF IN	Buffer Input
2, 8, 9, 14	NC	No Connection
3	COMMON	Analog Common
4	OUTPUT OFFSET	Output Offset
5	CS	Chip Select
6	DEN INPUT	Denominator Input
7	dB OUTPUT	dB Output
10	C_{AV}	Averaging Capacitor Connection
11	RMS OUT	RMS Output
12	$-V_S$	Negative Supply Rail
13	$+V_S$	Positive Supply Rail
15	V_{IN}	Signal Input
16	BUFF OUT	Buffer Output

FUNCTIONAL DESCRIPTION

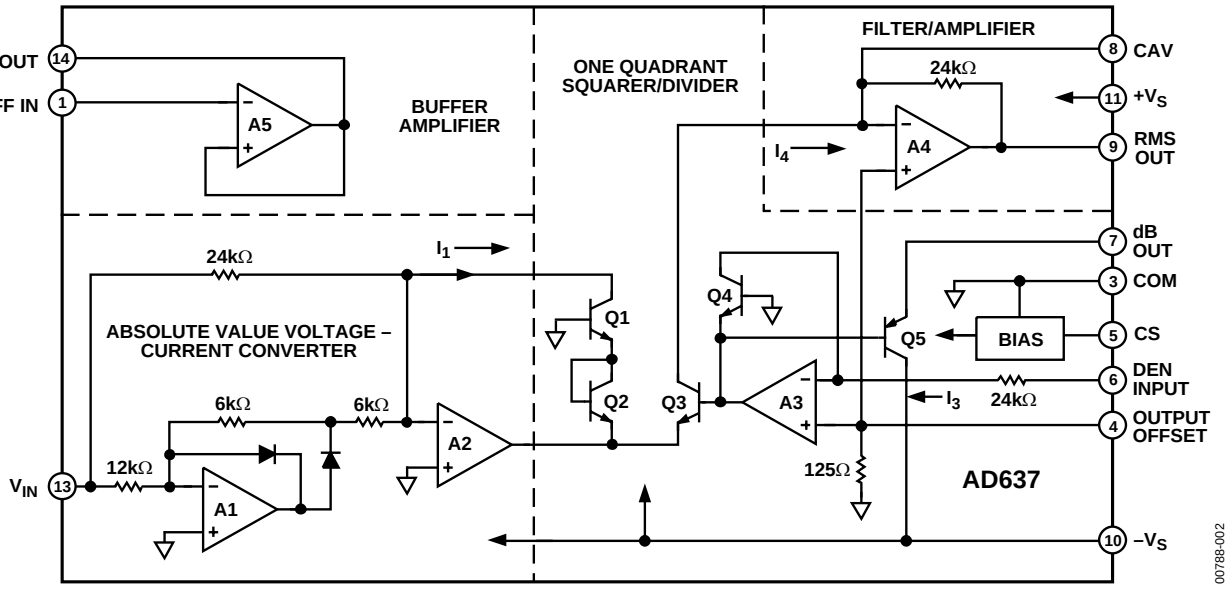


Figure 4. Simplified Schematic

The AD637 embodies an implicit solution of the rms equation that overcomes the inherent limitations of straightforward rms computation. The actual computation performed by the AD637 follows the equation

$$V\ rms = Avg\left[\frac{V_{IN}{}^2}{V\ rms}\right]$$

Figure 4 is a simplified schematic of the AD637, subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, filter circuit, and buffer amplifier. The input voltage V_{IN}, which can be ac or dc, is converted to a unipolar current I_1 by the active rectifier A1, A2. I_1 drives one input of the squarer/divider, which has the transfer function

$$I_4 = \frac{I_1^2}{I_3}$$

The output current of the squarer/divider I_4 drives A4, which forms a low-pass filter with the external averaging capacitor. If the RC time constant of the filter is much greater than the longest period of the input signal, A4's output is proportional to the average of I_4. The output of this filter amplifier is used by A3 to provide the denominator current I_3, which equals Avg I_4 and is returned to the squarer/divider to complete the implicit rms computation

$$I_4 = Avg\left[\frac{I_1^2}{I_4}\right] = I_1\ rms$$

and

$$V_{OUT} = V_{IN}\ rms$$

If the averaging capacitor is omitted, the AD637 computes the absolute value of the input signal. A nominal 5 pF capacitor should be used to ensure stability. The circuit operates identically to that of the rms configuration except that I_3 is now equal to I_4, giving

$$I_4 = \frac{I_1^2}{I_4}$$

$$I_4 = |I_1|$$

The denominator current can also be supplied externally by providing a reference voltage, V_{REF}, to Pin 6. The circuit operates identically to the rms case except that I_3 is now proportional to V_{REF}. Therefore,

$$I_4 = Avg\ \frac{I_1^2}{I_3}$$

and

$$V_O = \frac{V_{IN}{}^2}{V_{DEN}}$$

This is the mean square of the input signal.

STANDARD CONNECTION

The AD637 is simple to connect for a majority of rms measurements. In the standard rms connection shown in Figure 5, only a single external capacitor is required to set the averaging time constant. In this configuration, the AD637 computes the true rms of any input signal. An averaging error, the magnitude of which is dependent on the value of the averaging capacitor, is present at low frequencies. For example, if the filter capacitor, C_{AV}, is 4 µF, the error is 0.1% at 10 Hz and increases to 1% at 3 Hz. To measure ac signals, the AD637 can be ac-coupled through the addition of a nonpolar capacitor in series with the input, as shown in Figure 5.

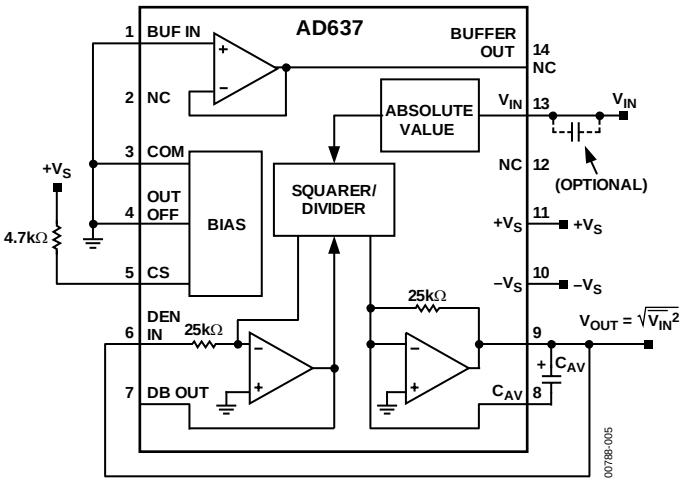


Figure 5. Standard RMS Connection

The performance of the AD637 is tolerant of minor variations in the power supply voltages; however, if the supplies used exhibit a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground through a 0.1 µF ceramic disc capacitor placed as close to the device as possible.

The output signal range of the AD637 is a function of the supply voltages, as shown in Figure 6. The output signal can be used buffered or nonbuffered, depending on the characteristics of the load. If no buffer is needed, tie the buffer input (Pin 1) to common. The output of the AD637 is capable of driving 5mA into a 2 kΩ load without degrading the accuracy of the device.

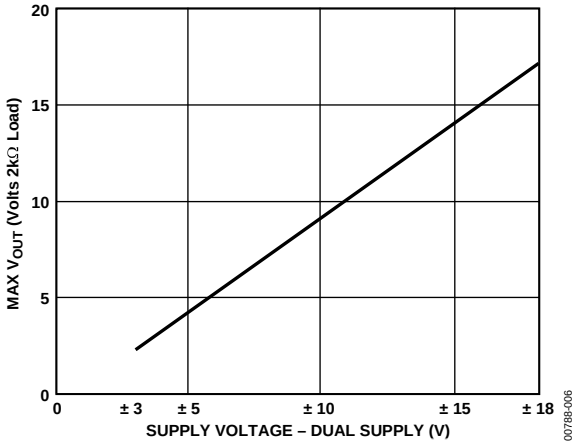


Figure 6. AD637 Maximum V_{OUT} vs. Supply Voltage

CHIP SELECT

The AD637 includes a chip select feature that allows the user to decrease the quiescent current of the device from 2.2 mA to 350 µA. This is done by driving the CS, Pin 5, to below 0.2 V dc. Under these conditions, the output goes into a high impedance state. In addition to lowering power consumption, this feature permits bussing the outputs of a number of AD637s to form a wide bandwidth rms multiplexer. If the chip select is not being used, Pin 5 should be tied high.

OPTIONAL TRIMS FOR HIGH ACCURACY

The AD637 includes provisions for trimming out output offset and scale factor errors resulting in significant reduction in the maximum total error, as shown in Figure 7. The residual error is due to a nontrimmable input offset in the absolute value circuit and the irreducible nonlinearity of the device.

Referring to Figure 8, the trimming process follows:

- Offset trim: Ground the input signal, V_{IN}, and adjust R1 to give 0 V output from Pin 9. Alternatively, R1 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
- Scale factor trim: Resistor R4 is inserted in series with the input to lower the range of the scale factor. Connect the desired full-scale input to V_{IN}, using either a dc or a calibrated ac signal, and trim R3 to give the correct output at Pin 9, that is, 1 V dc should give l.000 V dc output. Of course, a 2 V p-p sine wave should give 0.707 V dc output. Remaining errors are due to the nonlinearity.

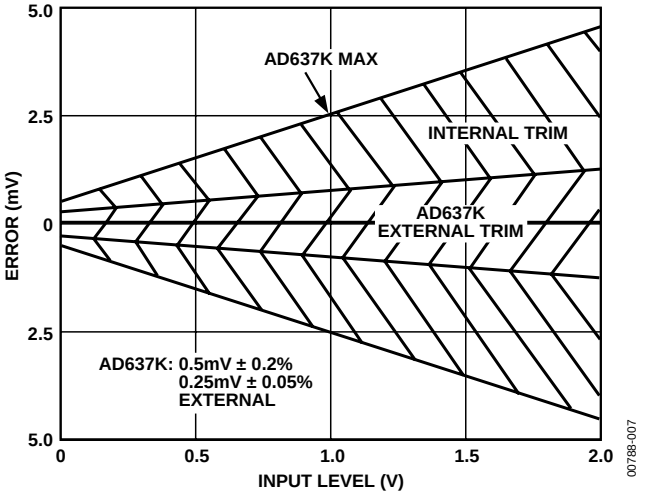


Figure 7. Maximum Total Error vs. Input Level AD637K Internal and External Trims

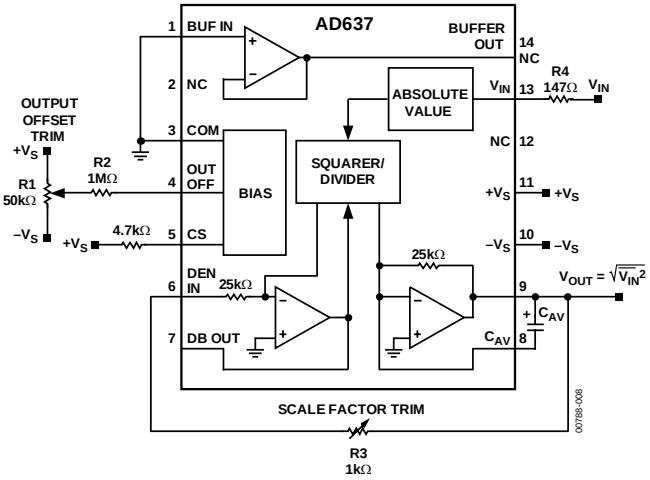


Figure 8. Optional External Gain and Offset Trims

CHOOSING THE AVERAGING TIME CONSTANT

The AD637 computes the true rms value of both dc and ac input signals. At dc, the output tracks the absolute value of the input exactly; with ac signals, the AD637's output approaches the true rms value of the input. The deviation from the ideal rms value is due to an averaging error. The averaging error is comprised of an ac and dc component. Both components are functions of input signal frequency f and the averaging time constant τ (τ: 25 ms/μF of averaging capacitance). Figure 9 shows that the averaging error is defined as the peak value of the ac component, ripple, and the value of the dc error.

The peak value of the ac ripple component of the averaging error is defined approximately by the relationship

$$\frac{50}{6.3\,\tau f}\ in\ \%\ of\ reading\ where\ (\tau > 1/f)$$

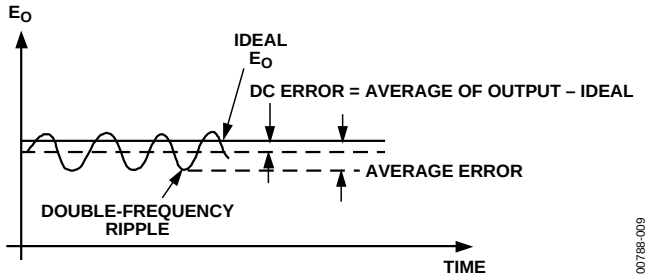


Figure 9. Typical Output Waveform for a Sinusoidal Input

This ripple can add a significant amount of uncertainty to the accuracy of the measurement being made. The uncertainty can be significantly reduced through the use of a post filtering network or by increasing the value of the averaging capacitor.

The dc error appears as a frequency dependent offset at the output of the AD637 and follows the equation

$$\frac{1}{0.16 + 6.4\,\tau^2 f^2}\ in\ \%\ of\ reading$$

Since the averaging time constant, set by C_{AV}, directly sets the time that the rms converter holds the input signal during computation, the magnitude of the dc error is determined only by C_{AV} and is not affected by post filtering.

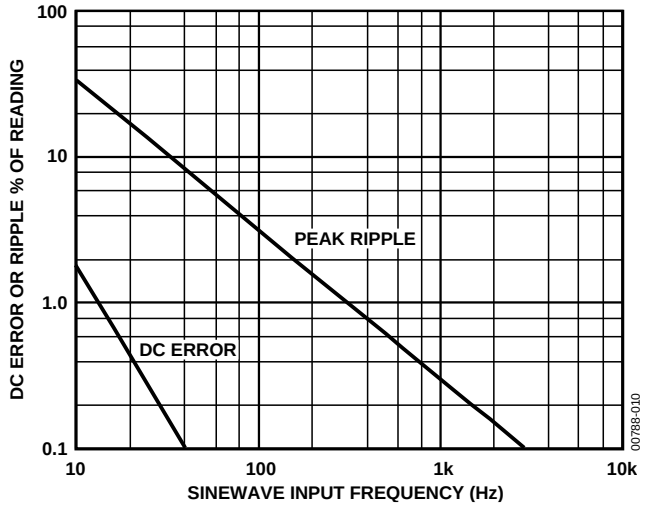


Figure 10. Comparison of Percent DC Error to the Percent Peak Ripple over Frequency Using the AD637 in the Standard RMS Connection with a 1 × μF C_{AV}

The ac ripple component of averaging error is greatly reduced by increasing the value of the averaging capacitor. There are two major disadvantages to this: the value of the averaging capacitor becomes extremely large and the settling time of the AD637 increases in direct proportion to the value of the averaging capacitor (Ts = 115 ms/μF of averaging capacitance). A preferable method of reducing the ripple is through the use of the post filter network, as shown in Figure 11. This network can be used in either a one-pole or two-pole configuration. For most applications, the single pole filter gives the best overall compromise between ripple and settling time.

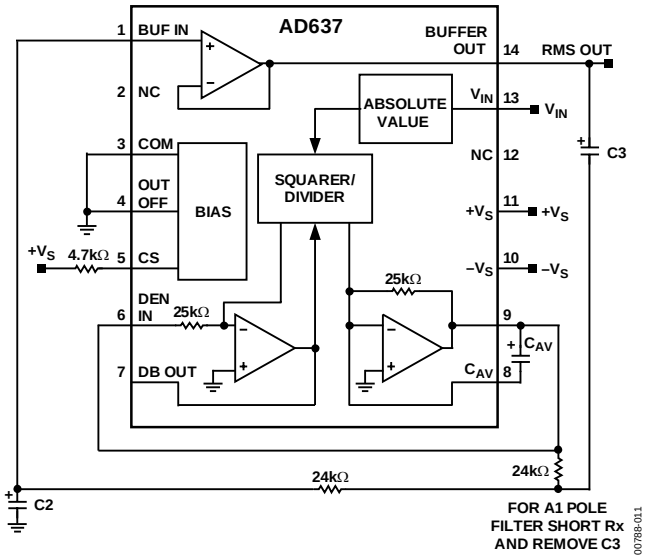


Figure 11. Two-Pole Sallen-Key Filter

Figure 12 shows values of C_{AV} and the corresponding averaging error as a function of sine wave frequency for the standard rms connection. The 1% settling time is shown on the right side of Figure 12.

Figure 13 shows the relationship between the averaging error, signal frequency settling time, and averaging capacitor value. Figure 13 is drawn for filter capacitor values of 3.3× the averaging capacitor value. This ratio sets the magnitude of the ac and dc errors equal at 50 Hz. As an example, by using a 1 µF averaging capacitor and a 3.3 µF filter capacitor, the ripple for a 60 Hz input signal is reduced from 5.3% of the reading using the averaging capacitor alone to 0.15% using the single-pole filter. This gives a factor of 30 reduction in ripple and yet the settling time only increases by a factor of 3. The values of C_{AV} and C2, the filter capacitors, can be calculated for the desired value of averaging error and settling time by using Figure 13.

The symmetry of the input signal also has an effect on the magnitude of the averaging error. Table 5 gives the practical component values for various types of 60 Hz input signals. These capacitor values can be directly scaled for frequencies other than 60 Hz; that is, for 30 Hz these values are doubled, for 120 Hz they are halved.

For applications that are extremely sensitive to ripple, the two-pole configuration is suggested. This configuration minimizes capacitor values and the settling time while maximizing performance.

Figure 14 can be used to determine the required value of C_{AV}, C2, and C3 for the desired level of ripple and settling time.

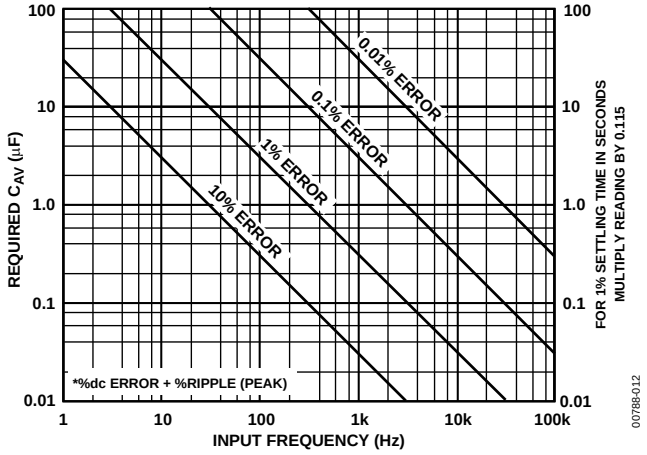


Figure 12. Values for C_{AV}, and 1% Settling Time for Stated % of Reading Averaging Error Accuracy Includes ±2% Component Tolerance (see * in Figure)*

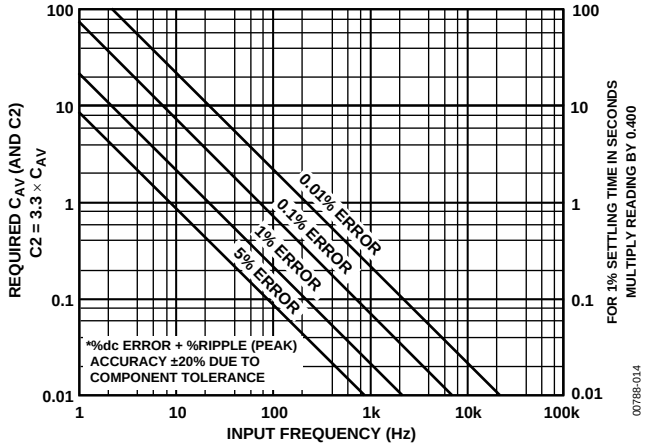


Figure 13. Values of C_{AV}, C2, and 1% Settling Time for Stated % of Reading Averaging Error for 1-Pole Post Filter (see * in Figure)*

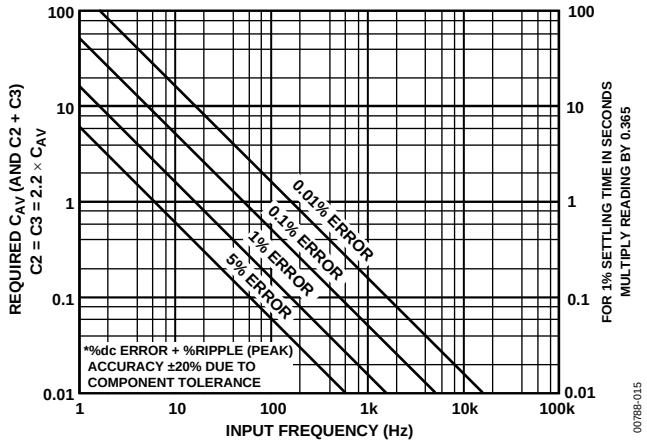
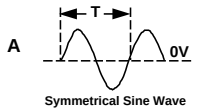
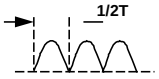
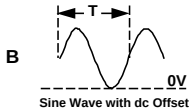
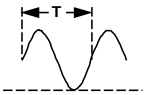
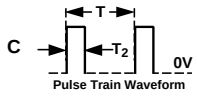
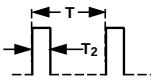
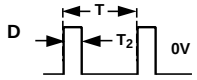
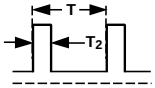


Figure 14. Values of C_{AV}, C2, and C3 and 1% Settling Time for Stated % of Reading Averaging Error 2-Pole Sallen-Key Filter (see * in Figure)*

Table 5. Practical Values of C_{AV} and C2 for Various Input Waveforms

Input Waveform and Period	Absolute Value Circuit Waveform and Period	Minimum R × C_{AV} Time Constant	Recommended C_{AV} and C2 Values for 1% Averaging Error @ 60 Hz with T = 16.6 ms		1% Settling Time
			Recommended Standard Value C_{AV}	Recommended Standard Value C2	
A 		1/2T	0.47 µF	1.5 µF	181 ms
B 		T	0.82 µF	2.7 µF	325 ms
C 		10 (T – T_2)	6.8 µF	22 µF	2.67 sec
D 		10 (T – 2T_2)	5.6 µF	18 µF	2.17 sec

FREQUENCY RESPONSE

The frequency response of the AD637 at various signal levels is shown in Figure 15. The dashed lines show the upper frequency limits for 1%, 10%, and ±3 dB of additional error. For example, note that for 1% additional error with a 2 V rms input, the highest frequency allowable is 200 kHz. A 200 mV signal can be measured with 1% error at signal frequencies up to 100 kHz.

To take full advantage of the wide bandwidth of the AD637, care must be taken in the selection of the input buffer amplifier. To ensure that the input signal is accurately presented to the converter, the input buffer must have a −3 dB bandwidth that is wider than that of the AD637. Note the importance of slew rate in this application. For example, the minimum slew rate required for a 1 V rms, 5 MHz, sine wave input signal is 44 V/µs. The user is cautioned that this is the minimum rising or falling slew rate and that care must be exercised in the selection of the buffer amplifier, since some amplifiers exhibit a two-to-one difference between rising and falling slew rates. The AD845 is recommended as a precision input buffer.

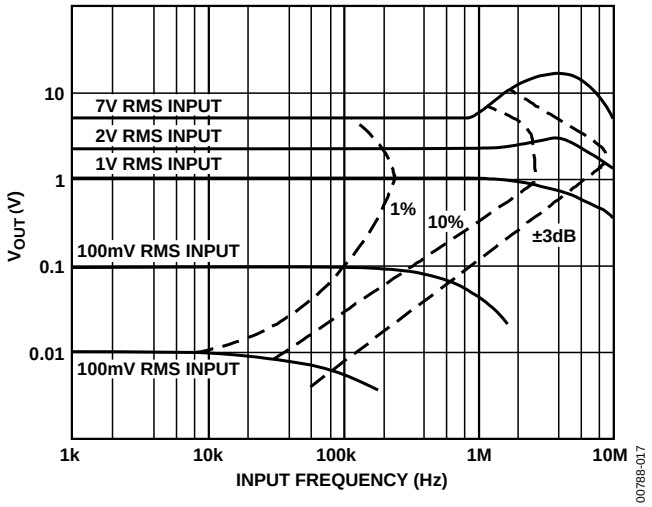


Figure 15. Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal (CF = Vp/V rms). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (≤2). Waveforms that resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (CF = $1\sqrt{\eta}$).

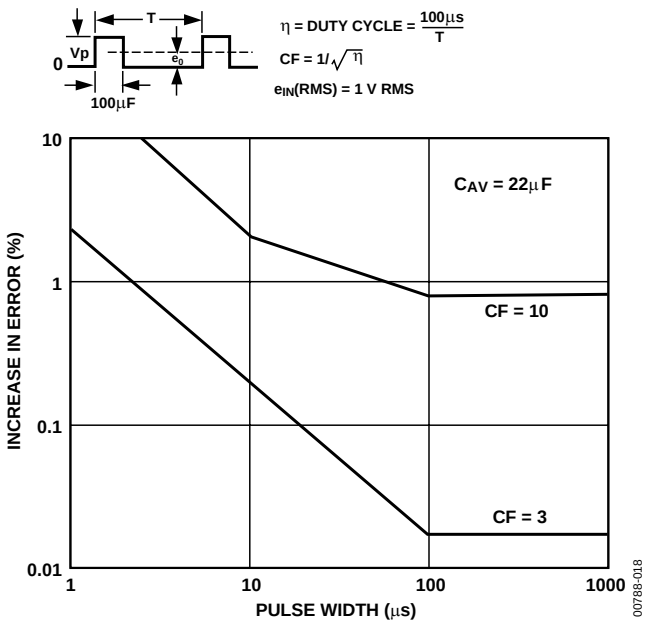


Figure 16. AD637 Error vs. Pulse Width Rectangular Pulse

Figure 17 is a curve of additional reading error for the AD637 for a 1 V rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100 μs) was used for this test because it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from l to 10 while maintaining a constant 1 V rms input amplitude.

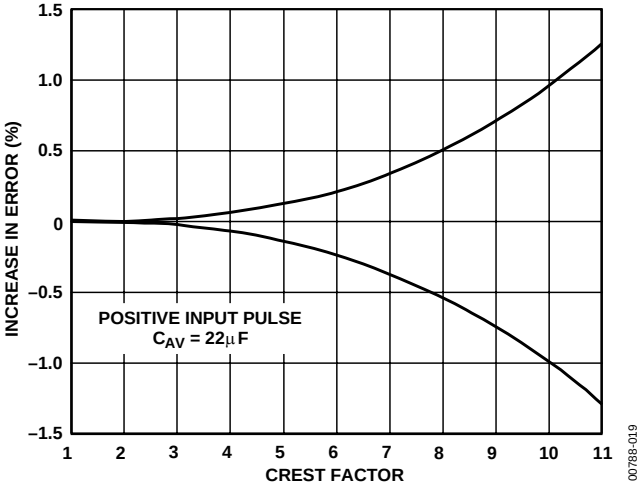


Figure 17. Additional Error vs. Crest Factor

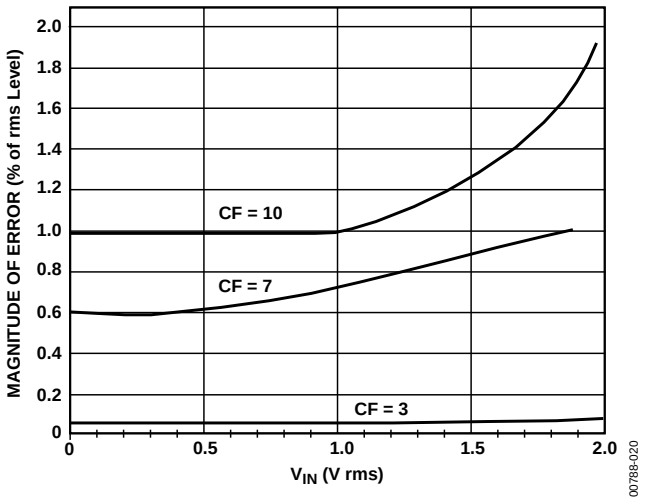


Figure 18. Error vs. RMS Input Level for Three Common Crest Factors

CONNECTION FOR DB OUTPUT

Another feature of the AD637 is the logarithmic, or decibel, output. The internal circuit that computes dB works well over a 60 dB range. Figure 19 shows the dB measurement connection. The user selects the 0 dB level by setting R1 for the proper 0 dB reference current, which is set to exactly cancel the log output current from the squarer/divider circuit at the desired 0 dB point. The external op amp is used to provide a more convenient scale and to allow compensation of the +0.33%/°C temperature drift of the dB circuit. The special TC resistor R3 is available from Precision Resistor Inc., Largo, Fla (Model PT146).

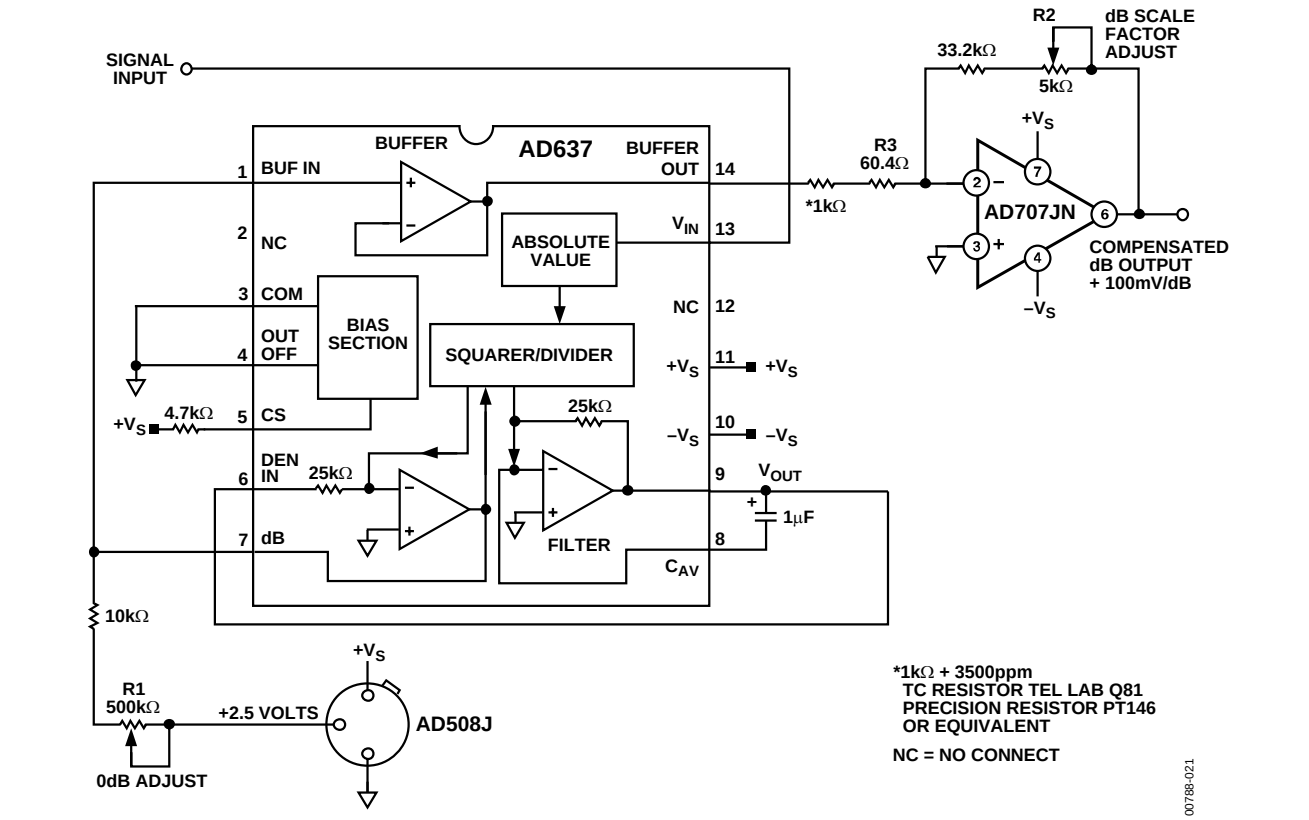


Figure 19. dB Connection

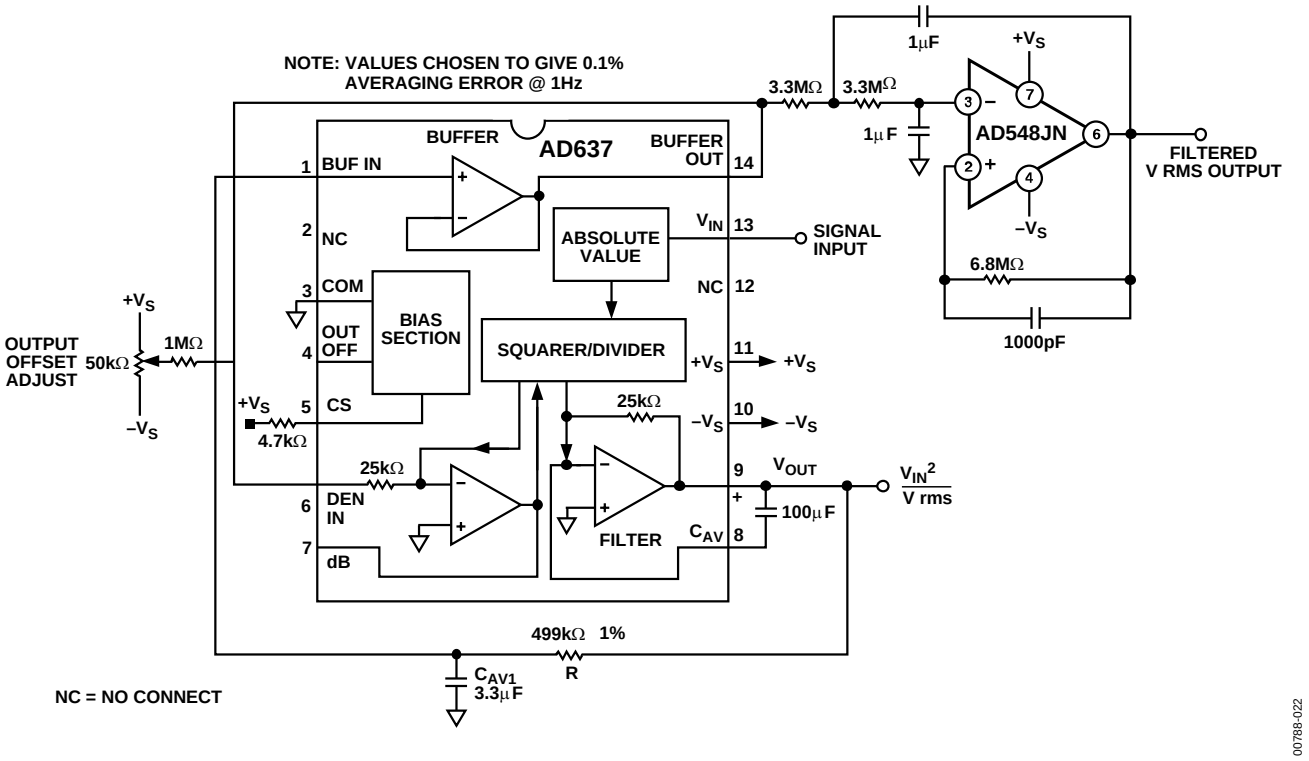


Figure 20. AD637 as a Low Frequency RMS Converter

dB CALIBRATION

Refer to Figure 19:

- Set VIN = 1.00 V dc or 1.00 V rms
- Adjust R1 for 0 dB out = 0.00 V
- Set VIN = 0.1 V dc or 0.10 V rms
- Adjust R2 for dB out = −2.00 V

Any other dB reference can be used by setting V_{IN} and R1 accordingly.

LOW FREQUENCY MEASUREMENTS

If the frequencies of the signals to be measured are below 10 Hz, the value of the averaging capacitor required to deliver even 1% averaging error in the standard rms connection becomes extremely large. Figure 20 shows an alternative method of obtaining low frequency rms measurements. The averaging time constant is determined by the product of R and C_{AV1}, in this circuit 0.5 s/µF of C_{AV}. This circuit permits a 20:1 reduction in the value of the averaging capacitor, permitting the use of high quality tantalum capacitors. It is suggested that the two-pole, Sallen-Key filter shown in Figure 20 be used to obtain a low ripple level and minimize the value of the averaging capacitor.

If the frequency of interest is below 1 Hz, or if the value of the averaging capacitor is still too large, the 20:1 ratio can be increased. This is accomplished by increasing the value of R. If this is done, it is suggested that a low input current, low offset voltage amplifier, such as the AD548, be used instead of the internal buffer amplifier. This is necessary to minimize the offset error introduced by the combination of amplifier input currents and the larger resistance.

VECTOR SUMMATION

Vector summation can be accomplished through the use of two AD637s, as shown in Figure 21. Here the averaging capacitors are omitted (nominal 100 pF capacitors are used to ensure stability of the filter amplifier), and the outputs are summed as shown. The output of the circuit is

$$V_O = \sqrt{V_X^2 + V_Y^2}$$

This concept can be expanded to include additional terms by feeding the signal from Pin 9 of each additional AD637 through a 10 kΩ resistor to the summing junction of the AD711 and tying all of the denominator inputs (Pin 6) together.

If C_{AV} is added to IC1 in this configuration, the output is

$$\sqrt{\overline{V_X^2} + V_Y^2}$$

If the averaging capacitor is included on both IC1 and IC2, the output is

$$\sqrt{\overline{V_X^2} + \overline{V_Y^2}}$$

This circuit has a dynamic range of 10 V to 10 mV and is limited only by the 0.5 mV offset voltage of the AD637. The useful bandwidth is 100 kHz.

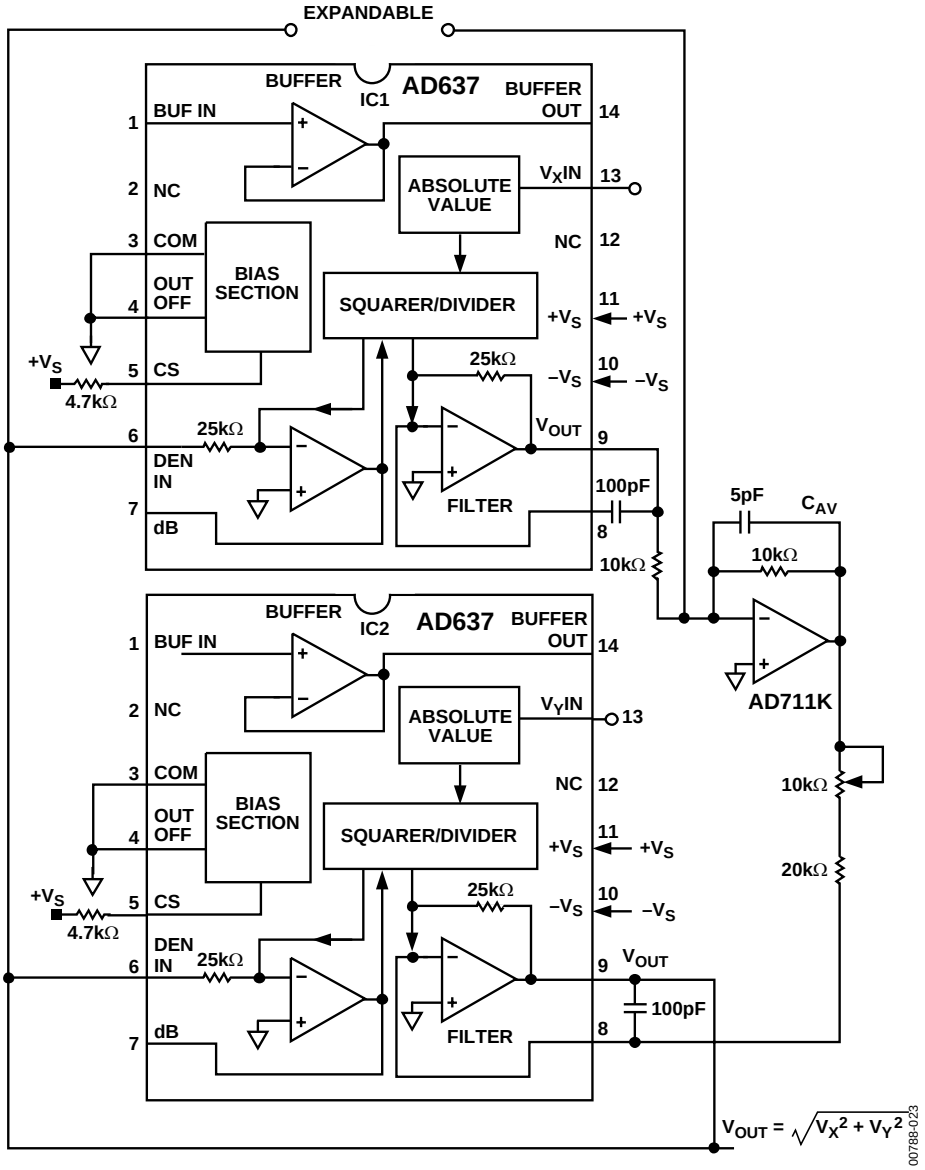
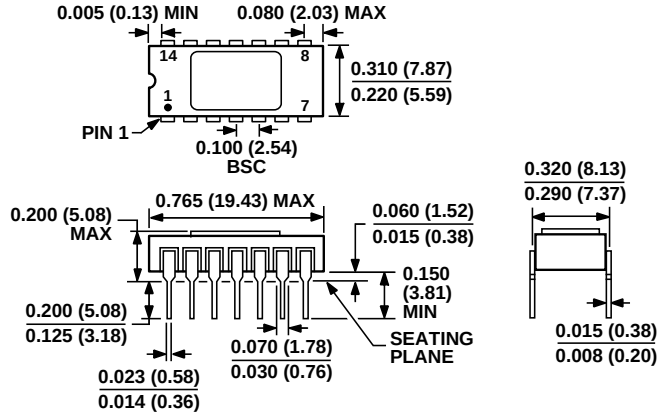


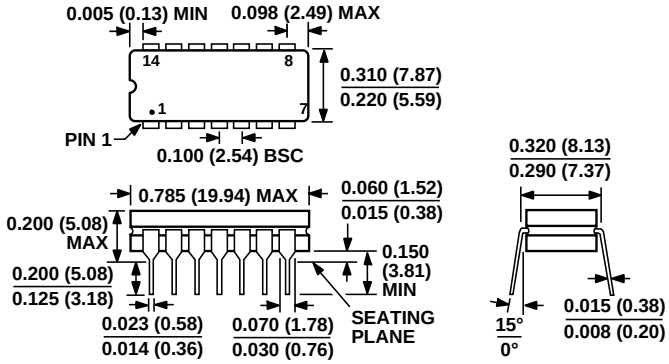
Figure 21. Vector Sum Configuration

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

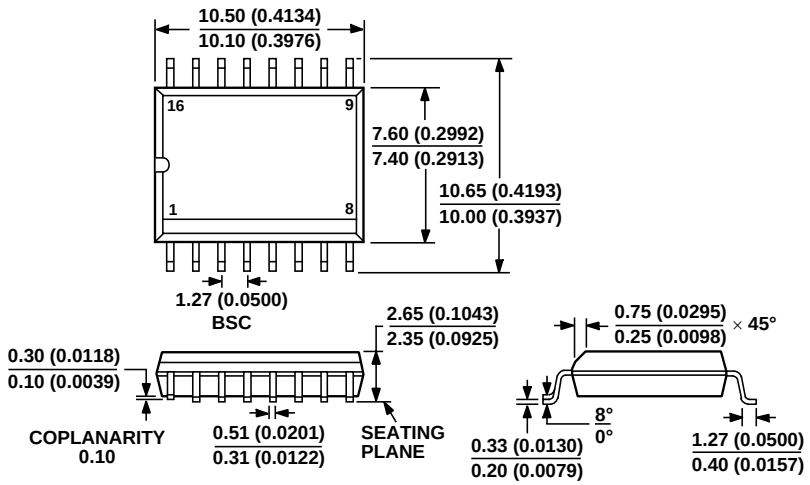
Figure 22. 14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]
(D-14)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 23. 14-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-14)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 24. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
5962-8963701CA[1]	−55°C to +125°C	14-Lead CERDIP	Q-14
AD637AQ	−40°C to +85°C	14-Lead CERDIP	Q-14
AD637AR	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD637BQ	−40°C to +85°C	14-Lead CERDIP	Q-14
AD637BR	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD637JD	0°C to 70°C	14-Lead SBDIP	D-14
AD637JQ	0°C to 70°C	14-Lead CERDIP	Q-14
AD637JR	0°C to 70°C	16-Lead SOIC_W	RW-16
AD637JR-REEL	0°C to 70°C	16-Lead SOIC_W	RW-16
AD637JR-REEL7	0°C to 70°C	16-Lead SOIC_W	RW-16
AD637JRZ[2]	0°C to 70°C	16-Lead SOIC_W	RW-16
AD637JRZ-R7[2]	0°C to 70°C	16-Lead SOIC_W	RW-16
AD637JRZ-RL[2]	0°C to 70°C	16-Lead SOIC_W	RW-16
AD637KD	0°C to 70°C	14-Lead SBDIP	D-14
AD637KQ	0°C to 70°C	14-Lead CERDIP	Q-14
AD637KR	0°C to 70°C	16-Lead SOIC_W	RW-16
AD637SD	−55°C to +125°C	14-Lead SBDIP	D-14
AD637SD/883B	−55°C to +125°C	14-Lead SBDIP	D-14
AD637SQ/883B	−55°C to +125°C	14-Lead CERDIP	Q-14

[1] A standard microcircuit drawing is available.
[2] Z = Pb-free part.

NOTES

NOTES

C00788–0–4/05(G)